

1                    **ABSTRACT OF THE DISCLOSURE**

2                    The invention comprises FLASH memory and methods of forming  
3                    flash memory. In one implementation, a line of floating gates is  
4                    formed over a semiconductor substrate. The semiconductor substrate is  
5                    etched to form a series of spaced trenches therein in a line adjacent  
6                    and along at least a portion of the line of floating gates. At least one  
7                    conductivity enhancing impurity implant is conducted into the  
8                    semiconductor substrate at an angle away from normal to a general  
9                    orientation of the semiconductor substrate to implant at least along  
10                    sidewalls of the trenches and between the trenches, and a continuous  
11                    line of source active area is formed within the semiconductor substrate  
12                    along at least a portion of the line of floating gates. In another  
13                    implementation, a line of floating gates is formed over a semiconductor  
14                    substrate. An alternating series of trench isolation regions and active  
15                    area regions are provided in the semiconductor substrate in a line  
16                    adjacent and along at least a portion of the line of floating gates.  
17                    The series of active areas define discrete transistor source areas  
18                    separated by trench isolation regions. A conductive line is formed over  
19                    the discrete transistor source areas and trench isolation regions  
20                    separating same adjacent and along at least a portion of the line of  
21                    floating gates. The conductive line electrically interconnects the discrete  
22                    transistor source areas. Source forming conductivity enhancing impurity  
23                    is provided into the discrete transistor source areas. Other  
24                    implementations are contemplated.